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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,841	11/13/2003	Rajesh Sundaram	ITL.1062US (P17921)	2553

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,841	SUNDARAM ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5,7,9-11,14-17,19,22-25,27-33,35,36 and 38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-11,14-17,19,31,35-36 and 38* is/are allowed.

6)☐ Claim(s) *1,3-5,7,9,22-25,27-30,32 and 33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Amendment filed on 05/26/2006 has been entered.

Claims 1,3-5,7,9-11,14-17,19,22-25,27-33,35-36,38 are presented for examination.

Response to Arguments

2. Applicant's arguments with respect to claims 1,3-5,7,9-11,14-17,19,22-25,27-33,35-36,38 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1,3-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Radjy et al. (U.S. Patent No. 5,579,261).

Regarding claim 1, Radjy et al. disclose a method (ABSTRACT) comprising:

supplying a negative voltage to at least one deselected wordline of a non-volatile memory array from a decoder coupled to the at least one deselected wordline during a programming operation on a selected wordline (Column 3, lines 60-67, Column 4, lines 1-5);

providing the negative voltage and a control negative voltage to the decoder (Figure 3, 204, it is inherent because a negative voltage supplied to unselected wordline form wordline decoder 204 in Figure 3); and

supplying a positive voltage to the selected wordline of the non-volatile memory array to program the selected wordline while supplying the negative voltage (Column 3, line 64-65, Column 4, lines 20-24, lines 49-50, Column 6, lines 47-49).

Regarding claim 3, Radjy et al. disclose supply the negative voltage to all wordlines of non-volatile memory array except the selected wordline (ABSTRACT, selected wordlines is applied a positive voltage, otherwise that unselected wordline is applied a negative voltage).

Regarding claim 4, Radjy et al. disclose further comprising proving a second positive voltage signal to a selected bitline of non-volatile memory array (Column 4, lines 49-52).

Regarding claim 5, Radjy et al. disclose further comprising reducing a leakage current (ABSTRACT through at least one deselected cell coupled to the selected bitline of the non- volatile memory array while programming the selected wordline, wherein the at least one deselected cell comprises a multi-level cell of a flash memory (Column 2, lines 31-58, memory cell in Figure 3 is a flash memory , column 1, lines 15-20).

5. Claims 1,3-4, 7,9, 22-25,27-30, 32-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Gill et al. (U.S. Patent No. 5,537,362).

Regarding claim 1, Gill et al. disclose a method (ABSTRACT) comprising:

supplying a negative voltage to at least one deselected wordline of a non-volatile memory array from a decoder coupled to the at least one deselected wordline during a programming operation on a selected wordline (ABSTRACT);

providing the negative voltage and a control negative voltage to the decoder (Figure 2, 30, Column 6, lines 12-25); and

supplying a positive voltage to the selected wordline of the non-volatile memory array to program the selected wordline while supplying the negative voltage (Column 5, lines 35-50, lines 59-62).

Regarding claim 3, Gill et al. disclose supply the negative voltage to all wordlines of non-volatile memory array except the selected wordline (Column 5, lines 25-50).

Regarding claim 4, Radjy et al. disclose further comprising proving a second positive voltage signal to a selected bitline of non-volatile memory array (Figure 2, 38).

Regarding claim 7, Gill et al. disclose further comprising providing the control negative voltage to a substrate of a transistor of the decoder coupled to pass the negative voltage to the at least one deselected wordline (Column 8, lines 63-67).

Regarding claim 9, Gill et al. disclose further supplying the negative voltage to the deselected wordline during a first time period, and supplying a positive voltage to the same wordline during a second time period to program at least one memory cell coupled thereto (Column 7, lines 43-63, Column 9, lines 65-67, Column 10, lines 1-13).

Regarding claim17, Gill et al. disclose an article comprising a machine-readable storage medium containing instructions that if executed enable a system to supply a negative voltage to at least one deselected wordline of a memory array; end provide a

negative control voltage to a substrate of a transistor coupled to pass the negative voltage to the at least one deselected wordline supply a positive voltage to a selected wordline of the memory array to program the selected wordline while the negative voltage is supplied to the at least one deselected wordline; and control a first pre-driver circuit coupled to the at least one deselected wordline to pass a positive control voltage to a first control node-coupled to a first pair of transistors of different polarities and to control a second pre-driver circuit coup-led to the selected wordline to discharge a second control node coupled to a second pair of transistors of different polarities.

Regarding claims 22, 30, Gill et al. disclose a system (Figure 5) comprising:

a nonvolatile memory array (Figure 5, 12) having a plurality of memory cells each coupled to a wordline and a bitline;

a decoder (Figure 5, 32 and 36) coupled to the nonvolatile memory array to supply a negative voltage to a deselected wordline of the nonvolatile memory array, wherein the decoder comprises a first transistor (Figure 5, 62) of a first polarity to pass the negative voltage to the deselected wordline and a second transistor (Figure 5, 62) of a second polarity coupled to the first transistor to pass a program voltage, if the deselected wordline becomes a selected wordline (Column 7, lines 43-51, Column 8, lines 14-21); and a wireless interface coupled to the nonvolatile memory array (it is inherent in prior art, since it is a optional).

Regarding claim 23, Gill et al. disclose wherein the decoder is further coupled to supply a positive voltage to the deselected wordline if it becomes a selected wordline (Column 7, lines 45-51, deselect 1023 word lines, place Vcc on the select word lines).

Regarding claim 24, Gill et al. disclose further comprising a second decoder to supply a positive voltage to a selected wordline while the negative voltage is supplied to the deselected wordline (Column 7, lines 47-51).

Regarding claim 25, Gill et al. disclose wherein the first transistor comprises a well coupled to receive a negative control voltage, a source terminal coupled to receive the negative voltage, and a drain terminal coupled to pass the negative voltage to the deselected wordline (Column 8, lines 13-21).

Regarding claim 27, Gill et al. disclose further comprising a pre- driver circuit (Figure 5, 36) to disable the first transistor if the deselected wordline becomes a selected wordline, wherein the pre-driver circuit comprises a transistor chain coupled to an intermediate node coupled to a gate terminal of the first transistor, wherein the transistor chain is to provide a ground potential to the intermediate node to disable the first transistor (Figure 3, 32, Figure 5, 62, Column 7, lines 43-51, Column 8, lines 13-21).

Regarding claims 28-29, Gill et al. disclose wherein the nonvolatile memory array comprises a flash memory (Column 1, lines 24-35).

Regarding claims 32-33, Gill et al. disclose a negative switch (Figure 3, 32) coupled to provide the negative voltage (Figure 5, 34) and a negative control voltage (Column 6, lines 19-24) to the decoder, and wherein the negative switch is coupled to further provide the negative voltage and the negative control voltage to a second decoder coupled to another wordline of the non-volatile memory array (Column 5, lines 35-50, Column 6, lines 12-25).

Allowable Subject Matter

6. Claims 10-11,14-17, 19,31,35-36,38 are allowed.

Claims 10-11,14-17, 19,31,35-36,38 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Radjy et al. (U.S. Patent No. 5,579,261), Gill et al. (U.s. Patent No. 5,537,362, and others, does not teach the claimed invention having an apparatus comprising: a decoder to supply a negative voltage to a deselected address line of a memory array, the decoder comprising a first transistor of a first polarity coupled to receive a negative control voltage and the negative voltage and to pass the negative voltage to the deselected address line, and a second transistor of a second polarity coupled to the first transistor and the deselected address line to pass a program pulse to the deselected address line if it becomes a selected address line. the decoder further comprising a pre-driver circuit to control an intermediate node coupled to a gate terminal of the first transistor and a, gate terminal of the second transistor as claims 10-11,14-16,31,35-36 disclosed, and supply a positive voltage to a selected wordline of the memory array to program the selected wordline while the negative voltage is supplied to the at least one deselected wordline; and control a first pre-driver circuit coupled to the at least one deselected wordline to pass a positive control voltage to a first control node-coupled to a first pair of transistors of different polarities and to control a second pre-driver circuit coup-led to the selected wordline to discharge a

second control node coupled to a second pair of transistors of different polarities as claims 17, 19, 38 disclosed.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thong Q. Le
Primary Examiner
Art Unit 2827

8/4/2006